# STIC Search Report
## EIC 1700

## STIC Database Tracking Number: 124012

| | |
|---|---|
| **TO: George A Goudreau**<br>**Location: REM 7A21**<br>**Art Unit : 1763**<br>**June 8, 2004**<br><br>**Case Serial Number: 09/669159** | **From: Kendra Mellerson**<br>**Location: EIC 1700**<br>**REM 4B28**<br>**Phone: 571-272-2516**<br><br>**Kendra.Mellerson@uspto.gov** |

## Search Notes

No Cases Reported

US 6,283,131

# SEARCH REQUEST FORM

Requestor's Name: George Goudreau

Serial Number: 10-650,886

Date: 6-7-04 Phone: 571-272-1434 Art Unit: 1763

**Search Topic:**

Please write a detailed statement of search topic. Describe specifically as possible the subject matter to be searched. Define any terms that may have a special meaning. Give examples or relevent citations, authors, keywords, etc., if known. For sequences, please attach a copy of the sequence. You may include a copy of the broadest and/or most relevent claim(s).

Litigation search of US patent 6,046,109 which corresponds to US application 08-998,734, (for reissue)

## STAFF USE ONLY

Date completed: _____

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Terminal time: _____

Elapsed time: _____

CPU time: _____

Total time: _____

Number of Searches: _____

Number of Databases: _____

**Search Site**

_____ STIC

_____ CM-1

_____ Pre-S

**Type of Search**

_____ N.A. Sequence

_____ A.A. Sequence

_____ Structure

Bibliographic

**Vendors**

_____ IG

_____ STN

_____ Dialog

_____ APS

_____ Geninfo

_____ SDC

_____ DARC/Questel

Other

# Current session 08/06/2004

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## Query/Command : FILE PLUSPAT

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Search statement 1

## Query/Command : US6283131/PN

** SS 1: Results 1

Search statement 2

## Query/Command : PRT FULL NONSTOP LEGALALL

*1 / 1 PLUSPAT - ©QUESTEL-ORBIT*

**PN** - US6283131 B1 20010904 [US6283131]

**TI** - (B1) In-situ strip process for polysilicon etching in deep sub-micron technology

**PA** - (B1) TAIWAN SEMICONDUCTOR MFG (US)

**PA0** - Taiwan Semiconductor Manufacturing Company, Hsin-Chu [TW]

**IN** - (B1) CHEN HORNG-WEN (TW); WU CHI-HOW (TW)

**AP** - US66915900 20000925 [2000US-0669159]

**PR** - US66915900 20000925 [2000US-0669159]

**IC** - (B1) H01L-021/302

**EC** - H01L-021/3213D

**PCL** - ORIGINAL (O) : 134001200; CROSS-REFERENCE (X) : 257E21314 438725000

**DT** - Basic

**CT** - US5346586; US5382316; US5767018; US5804088; US5885902; US5976769; US6037266; US6130166

**STG** - (B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001

**AB** - A new method of patterning the polysilicon layer in the manufacture of an integrated circuit device has been achieved. A polysilicon layer is provided overlying a semiconductor substrate. The polysilicon layer may overlie a gate oxide layer and thereby comprise the polysilicon gate for MOS devices. A hard mask layer is provided overlying the polysilicon layer. A resist layer is provided overlying the hard mask layer. The resist layer is patterned to form a resist mask the exposes a part of the hard mask layer. The polysilicon layer is patterned in a plasma dry etching chamber. First, the resist layer is optionally trimmed by etching. Second, the hard mask layer is etched where exposed by the resist mask to form a hard mask that exposes a part of the polysilicon layer. Third, the resist mask is stripped away. Fourth, polymer residue from the resist mask is cleaned away using a chemistry containing CF4 gas. Fifth, the polysilicon layer is etched where exposed by the hard mask. After the polysilicon layer is so patterned in the dry plasma etch chamber, the hard mask layer is stripped away to complete the patterning of the polysilicon layer in the manufacture of the integrated circuit device.

**UP** - 2001-37

*1 / 1 LGST - ©EPO*

**PN** - US6283131 B1 20010904 [US6283131]

**AP** - US66915900 20000925 [2000US-0669159]

**ACT** - 20031125 US/RF-A
REISSUE APPLICATION FILED
EFFECTIVE DATE: 20030828

**UP** - 2003-49

*1 / 1 CRXX - ©CLAIMS/RRX*

**PN** - 6,283,131 A 20010904 [US6283131]
**PA** - Taiwan Semiconductor Manufacturing Co TW
**ACT** - 20030828 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20031125
REISSUE REQUEST NUMBER: 10/650886
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 1763

Reissue Patent Number:

Query/Command : FILE INPADOC

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PLUSPAT      - Time in minutes :   0,41
The cost estimation below is based on Questel's
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                              Estimated cost :    0.99 USD
Records displayed and billed   :      1
                              Estimated cost :    1.32 USD
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LGST         - Time in minutes :   0,02
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                              Estimated cost :    0.60 USD
Legal-Status informations       :      1
                              Estimated cost :    0.50 USD
Cost estimated for the last database search :    1.12 USD
Estimated total session cost                :    4.05 USD

CRXX         - Time in minutes :   0,03
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                              Estimated cost :    0.05 USD
Records displayed and billed   :      1
                              Estimated cost :    5.50 USD
Legal-Status informations       :      1
                              Estimated cost :    0.50 USD
Cost estimated for the last database search :    6.05 USD
Estimated total session cost                :   10.10 USD

LITA         - Time in minutes :   0,01
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Search statement   1
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Query/Command : FAM US6283131/PN

1 Patent Groups

** SS 1: Results 1

Search statement 2

Query/Command : FAMSTATE NONSTOP

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*1/1 INPADOC - ©INPADOC*

**PN** - US 6283131 BA 20010904 [US6283131]
**TI** - In-situ strip process for polysilicon etching in deep sub-micron technology
**IN** - CHEN HORNG-WEN [TW]; WU CHI-HOW [TW]
**PA** - TAIWAN SEMICONDUCTOR MFG [US]
**AP** - US 669159/00-A 20000925 [2000US-0669159]
**PR** - US 669159/00-A 20000925 [2000US-0669159]
**IC** - H01L-021/302

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*1/1 LEGALI - ©EPO*

**PN** - US6283131 B1 20010904 [US6283131]
**AP** - US66915900 20000925 [2000US-0669159]
**ACTE** - 20031125 US/RF-A
REISSUE APPLICATION FILED
EFFECTIVE DATE: 20030828
**UP** - 2003-49

PATNO IS 6283131

DATE: JUNE 8, 2004
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FILE: ALL

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PATNO IS 6283131

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LEVEL 1... 1

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LEVEL 1 - 1 PATENT

1. 6283131 , September 4, 2001 , In-situ strip process for polysilicon etching in deep sub-micron technology, Chen, Horng-Wen - Taichung, Taiwan (TW); Wu, Chi-How - Tainan, Taiwan (TW), 669159 (09), Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan (TW), 03, September 25, 2000 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY SCIENCE-BASED INDUSTRIAL PARK 121 PARK AVE. 3 HSIN- CHU R.O.C. TAIWAN, Reel and Frame Number: 011182/0578

CORE TERMS: layer, polysilicon, mask, etch, resist, chamber, photoresist, plasma, sccm, dry ...

LEVEL 1 - 1 OF 1 PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

6283131

<=1> Get Drawing Sheet 1 of 7

September 4, 2001

# In-situ strip process for polysilicon etching in deep sub-micron technology

REISSUE: August 28, 2003 - Reissue Application filed Ex. Gp.: 1763; Re. S.N. 10/650,886 (O.G. November 25, 2003)

APPL-NO: 669159 (09)

FILED-DATE: September 25, 2000

GRANTED-DATE: September 4, 2001

CORE TERMS: layer, polysilicon, mask, etch, resist, chamber, photoresist, plasma, sccm, dry ...

6283131 OR 6,283,131

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